AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth below:

1-10. (Cancelled without prejudice)

11. (Original) An apparatus, comprising:

a plurality of input latch banks; and

a configurable enabling pulse clock generator coupled to the plurality of input latch banks to configurably generate enabling pulse clocks for the plurality of input latch banks for a configurably selected one of a first and a second signaling mode.

12. (Original) The apparatus of claim 11, wherein the first signaling mode is a differential signaling mode, and the second signaling mode is a single-ended signaling mode.

13. (Original) The apparatus of claim 11, wherein

the plurality of input latch banks comprise 2n latch banks; and

the configurable enabling pulse clock generator comprises a first and a second configurable ring counter arrangement, each coupled to a different n of the latch banks, to jointly generate 2n enabling pulse clocks in a selected one of 2n points in time of a period when the apparatus is configured to operate in the first signaling mode, one enabling pulse clock for each point in time, and n points in time of the period when the apparatus is configured to operate in the second signaling mode, two enabling pulse clocks for each point in time.

14. (Original) The apparatus according to claim 11, wherein the apparatus further comprises a first and a second set of sense amplifier circuit configurably coupled to the

configurable enabling pulse clock generator for the first and the second signaling mode respectively, to provide the configurable enabling pulse clock generator with a first and a second strobe signal in accordance with the first and the second signaling mode respectively, on which, the configurable enabling clock pulse generator bases its generation of the enabling pulse clocks for the plurality of input latch banks.

15. (Original) The apparatus according to claim 14, wherein

the first set of sense amplifier circuit comprises a first and a second sense amplifier configurably coupled to the configurable enabling pulse generator to provide the configurable enabling pulse generator with the first and second strobe signals for the first signaling mode; and

the second set of sense amplifier circuit comprises a third and a fourth sense amplifier configurably coupled to the configurable enabling pulse generator to provide the configurable enabling pulse generator with the first and second strobe signals for the second signaling mode.

16. (Original) The apparatus according to claim 15, wherein the first set of sense amplifier circuit further comprises a squelching arrangement disposed in between the first and second sense amplifiers and the configurable enabling pulse clock generator to ensure correct provision of the first and second strobe signals to the configurable enabling pulse generator, the squelching arrangement including a squelch detector having a stop input that allows an external data provision source to denote a last valid strobe crossing edge.

17. (Original) The apparatus of claim 11, wherein the apparatus is a selected one of a microprocessor and a chipset.

18. (Original) A method comprising:

generating a plurality of enabling pulse clocks for a selected one of a first and a second signaling mode, employing a configurable enabling pulse clock generator configurable to generate the enabling pulse clocks for the selected one of the first and second signaling modes; and

latching a plurality of data bits based at least in part on the enabling pulse clocks.

19. (Original) The method of claim 18, wherein said generating comprises generating 2n enabling pulse clocks in a selected one of 2n points in time of a period when generating the enabling pulse clocks for the first signaling mode, one enabling pulse clock for each point in time, and n points in time of the period when generating the enabling pulse clocks for the second signaling mode, two enabling pulse clocks for each point in time.

20. (Original) The method according to claim 18, wherein the method further comprises providing a first and a second strobe signal for use to generate the enabling pulse clocks, configurably selected from outputs of a first and a second set of sense amplifier circuit.

21. (Original) A system, comprising:

an integrated circuit having an input section, including

a plurality of input latch banks; and

a configurable enabling pulse clock generator coupled to the plurality of input latch banks to configurably generate enabling pulse clocks for the plurality of input latch banks for a configurably selected one of a first and a second signaling mode;

a bus coupled to the integrated circuit; and

a networking interface coupled to the bus.

22. (Original) The system of claim 21, wherein the bus is coupled to the integrated circuit at least in part through the input section, and the first and second signaling modes are a differential signaling mode, and a single-ended signaling mode respectively.

23. (Original) The system of claim 21, wherein

the plurality of input latch banks comprise 2n latch banks; and

the configurable enabling pulse clock generator comprises a first and a second configurable ring counter arrangement, each coupled to a different n of the latch banks, to jointly generate 2n enabling pulse clocks in a selected one of 2n points in time of a period when the IC is configured to operate in the first signaling mode, one enabling pulse clock for each point in time, and n points in time of the period when the IC is configured to operate in the second signaling mode, two enabling pulse clocks for each point in time.

24. (Original) The system according to claim 21, wherein the system further comprises a first and a second set of sense amplifier circuit configurably coupled to the configurable enabling pulse clock generator for the first and the second signaling mode respectively, to provide the configurable enabling pulse clock generator with a first and a second strobe signal in accordance with the first and the second signaling mode respectively, on which, the configurable enabling clock pulse generator bases its generation of the enabling pulse clocks for the plurality of input latch banks.

25. (Original) The system according to claim 24, wherein

the first set of sense amplifier circuit comprises a first and a second sense amplifier configurably coupled to the configurable enabling pulse generator to provide the configurable enabling pulse generator with the first and second strobe signals for the first signaling mode; and

the second set of sense amplifier circuit comprises a third and a fourth sense amplifier configurably coupled to the configurable enabling pulse generator to provide

the configurable enabling pulse generator with the first and second strobe signals for the second signaling mode.

26. (Currently amended) The system of claim ~~1~~21, wherein the IC is a selected one of a microprocessor and a chipset.

27. (Original) The system of claim 21, wherein the system is a selected one of a wireless mobile phone, a personal digital assistant, a CD player, a DVD player, a digital camera, a set-top box and an entertainment control unit.